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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 9

Application Number: 09/620,649
Filing Date: July 20, 2000
Appellant(s): Cetin Kaya

MAILED
JUN 24 2002
GROUP 2800

Jay M. Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed September 28, 2001.

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(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

Applicant's statement that there are no known related appeals and/or interferences is acknowledged.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

No amendment after final has been filed.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

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(7) *Grouping of Claims*

The Brief contains a statement that all the claims on appeal stand or fall together.

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

6,051,467	Chan et al.	4-2000
5,926,711	Woo et al.	7-1999
6,001,689	Van Buskirk et al.	12-1999

(10) *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

Claims 12, 13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Van Buskirk et al., U. S. Patent 6,001,689.

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Van Buskirk et al. disclose an integrated circuit comprising a floating gate memory array wherein the array comprises a plurality of gate stacks having a channel dielectric (61, 62, 63), a polysilicon floating gate (51, 52, 53), a dielectric region disposed outwardly from the floating gate (71, 72, 73), and a polysilicon gate electrode (41, 42, 43) and a plurality of dielectric isolation regions disposed between the gate stacks (26, 27, 28, and 29), see Fig. 2A and column 4, lines 1-10). The structure further comprises trenches and moats (Fig. 7A) formed between the stacks (column 5, lines 35-55). First oxide spacers (120-125) and oxide layer (101) are formed between the gate stacks and subsequently planarized to expose the polysilicon gate (41, 42, 43)(column 5, lines 35-65).

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al (U.S. Patent 6,001,689) in view of Woo et al. (U.S. Patent 5,926,711).

Van Buskirk et al. is applied as above. Van Buskirk et al. lacks anticipation only of using hemispherical grains of silicon as the floating gate. Woo et al. teach a floating gate transistor wherein the floating gate (24C) is formed of amorphous silicon which is converted to hemispherical grains of silicon (Fig. 3F and column 4, lines 35-55). It would have been obvious to one of ordinary skill in the art to use a floating gate having hemispherical grains of silicon in order to improve the capacitive coupling of the floating and control gates.

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Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al. (U.S. Patent 6,001,689) in view of Chan et al. (U.S. Patent 6,051,467).

Van Buskirk et al. is applied as above. Van Buskirk et al. lacks anticipation only of the thickness of the oxide layer in the ONO intergate dielectric. Chan et al. teach that a typical thickness for the oxide layer in an ONO intergate dielectric is between 50 and 100 angstroms (column 3, lines 40-50). It would have been obvious to one skilled in the art to use an oxide layer having a thickness of 50 to 100 angstroms in the known method of Van Buskirk et al. because it is well known to do so, as evidenced by Chan et al., and because this oxide layer thickness provides sufficient gate separation and capacitive coupling. Further, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed thicknesses because Applicant has not disclosed that the claimed thicknesses are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using thicknesses other than those claimed. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

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(11) Response to Argument

Appellant has attempted to antedate the Van Buskirk Patent by arguing that a conception and reduction to practice with diligence from conception to the reduction to practice is present in this case. Appellant has alternately argued that the filing of his provisional application provided a constructive reduction to practice for a parent application to be subsequently filed or at least provided diligence after a conception with the filing of the parent of the subject application being either a constructive reduction to practice or a first constructive reduction to practice after conception with diligence (diligence being the filing and continued pendency of the provisional application. It has been well established that a previously abandoned application which was not pending with a subsequently filed application is evidence only of conception. An abandoned application with which no subsequent application was copending serves to abandon benefit of the application's filing as a constructive reduction to practice and the abandoned application is evidence only of conception. "While the filing of the original application theoretically constituted a constructive reduction to practice at the time, the subsequent abandonment of that application also resulted in an abandonment of the benefit of that filing as a constructive reduction to practice. The filing of the original application is, however, evidence of conception of the invention." *In re Costello* 219 USPQ 389, 392 (Fed. Cir. 1983). Hence, Appellant can only rely on the filing of the provisional application under 35 USC 119(e) as evidence of conception.

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Reduction to practice may be an actual reduction or a constructive reduction to practice which occurs when a patent application on the claimed invention is filed. When conception occurs prior to the date of the reference, but reduction to practice is afterward, it is not enough merely to allege that Appellant had been diligent. *Ex parte Hunter* 1889 C.D. 218; 49 O.G. 733 (Comm'r Pat. 1889). Rather, Appellant must show evidence of facts establishing diligence. Under 37 C.F.R. 1.131, the critical period in which diligence must be shown begins just prior to the effective date of the reference and ends with the date of reduction to practice, either actual or constructive (i.e., the filing of a United States patent application). In this case, diligence must be shown for the period of time which begins just prior to the effective filing date of the Van Buskirk et al. Patent and ends on the filing date of Appellant's parent application, the filing of which constitutes a constructive reduction to practice. The entire period during which diligence is required must be accounted for by either affirmative acts or acceptable excuses. Appellant's statement that there was no lack of diligence and reliance on the decision in *Keizer v. Bradley* 123 USPQ 215, 216 (CCPA 1959) wherein it is stated that "'attorney-diligence' and engineering-diligence'...does not require that an 'inventor or his attorney...drop all other work and concentrate on the particular invention involved'" is not a showing but a mere pleading. Moreover, diligence must be shown from just prior to the effective filing date of the Van Buskirk et al. Patent (January 16, 1998) to Appellant's constructive reduction to practice, that is, the filing of parent application Serial

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No. 09/168,047 on October 7, 1998, and not only for the seven day period from the date of abandonment of Appellant's provisional application to the filing of the parent application.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,




M. Wilczewski

MW

December 6, 2001

Conferees

Olik Chaudhuri 

Carl Whitehead, Jr. 